REMARKS

The foregoing amendment amends claims 1, 8-11, 16 and 19-26, and adds claims 27-33. Pending in the application are claims 1-33 of which claims 1, 16 and 19-27 are independent. The following comments address all stated grounds for rejection and place the presently pending claims, as identified above, in condition for allowance.

Claim Amendments

Claims 1, 8-11, 16 and 19-26 have been amended to clarify the scope of the claimed invention. In particular, Applicants have amended Claims 1, 16 and 19-26 to recite "a description of a finite state machine, the description including a temporal logic operator for defining a temporal logic condition." No new matter is added.

Claim Objections

Claim 8 is objected to because the terms "--event E--" and "--threshold T--" are unclear. In response to the objections, Applicants have amended claims 8-11 to change "--event E--" and "--threshold T--" to "-- symbols (E)--" and "--threshold (T)--", respectively. In light of the claim amendments, Applicants request the Examiner withdraw the objection of claim 8.

Claim Rejections Under 35 U.S.C. 102

Claims 1-26 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,581,191 to Schubert *et al.* ("Schubert"). Applicants respectfully traverse the rejection for the following reasons.

Claim 1 recites a method for operating a computer system. In the method, a description of a finite state machine is received in the system wherein the description includes a temporal logic operator for defining a temporal logic condition. Code is generated for emulating the described finite state machine. Claims 19-26 are directed to computer programming system claims or computer software product claims that recite similar limitations.

Schubert relates to debugging fabricated hardware designs at a Hardware Description Language (HDL) level. Schubert discloses that the hardware designs fabricated within

integrated circuit products are debugged at the HDL level using the limited input/output pins of the products.

Applicants respectfully submit that the cited reference fails to disclose each and every element of the claimed invention. Applicants submit that Schubert does not disclose *a description of a finite state machine, the description including a temporal logic operator for defining a temporal logic condition*, as recited in claim 1. In the claimed invention, users are able to describe a finite state machine using a temporal logic operator for defining a temporal logic condition. That is, the temporal logic operator is incorporated into the description of the finite state machine for defining the temporal logic condition in the claimed invention. The Examiner indicates in the Office Action that Schubert discloses this feature in Fig. 11 and at column 32, lines 35-67. Applicants respectfully disagree.

Schubert discloses in Fig. 1 that the instrumentor (110) receives an original HDL description (108) and generates an instrumented HDL description (112) to include a design instrumentation circuit (DIC) within the design under test (DUT). The instrumented HDL description represents not only the DUT but also the DIC. The debuggers are able to communicate with the DUT in order to debug the DUT fabricated within integrated circuit products.

Schubert also discloses a to-be-instrumented finite state machine (1102) as the DUT in Fig. 11. The finite state machine is coupled to a design control circuit (1100) that is added as a portion of the DIC. The design control circuit detects a particular state in the finite state machine and generates *a trigger condition signal (1118) to denote trigger events* (See, column 35, lines 2-38). In Fig. 11, Schubert does not disclose a description of a finite state machine (1102) that includes a temporal logic operator for defining a temporal logic condition.

In Fig. 8, Schubert discloses that the DIC includes a trigger processing unit (808) for processing trigger events and issuing trigger actions (See, column 32, lines 40-43). Schubert also discloses that *temporal logic may be used to describe the correspondence between the trigger events and the trigger actions* (See, column 32, lines 45-48). Accordingly, Schubert discloses that the trigger processing unit, which may include temporal logic, receives the trigger condition signal from the design control circuit (1100) depicted in Fig. 11 and processes the trigger

condition signal to issue trigger actions using, for example, the temporal logic. As a result, Schubert does not disclose that the finite state machine (1102) includes a temporal logic operator for defining a temporal logic condition, as recited in claim 1.

Schubert confirms this in Fig. 14 and corresponding description at column 37, lines 7-18. Schubert discloses a design control circuit (1400) that can be used to implement temporal logic. The design control circuit (1400) receives a trigger condition signal (1402) and generate an output (1416) that can be used as an input to temporal logic equations (See, column 37, lines 7-18). That is, the trigger control signal (1118) generated from the design control circuit (1100) depicted in Fig. 11 may be used as an input to temporal logic equations. Accordingly, Schubert does not disclose that the finite state machine (1102) depicted in Fig. 11 includes a temporal logic operator.

Additionally, Applicants submit that Schubert does not disclose *receiving* in the system a description of a finite state machine that includes a temporal logic operator, as recited in claim 1. Schubert discloses that the trigger processing unit (808), which may include temporal logic, is generated by the instrumentor (102) in the debugging system (100). In contrast, the claimed invention *receives* in the system a description of a finite state machine that includes a temporal logic operator. Schubert does not disclose *receiving* in the system a description of a finite state machine that includes a temporal logic operator.

In light of the aforementioned arguments, Applicants respectfully submit that Schubert fails to disclose each and every element of claims 1, 16 and 19-26. Applicants therefore request the Examiner withdraw the rejections of claims 1-26 under 35 U.S.C. §102(e), and pass the claims to allowance.

New claims

New claims 27-33 are added to clarify the scope of the claimed invention. New claims recite, at least in part, incorporating a temporal logic operator into the graphical representation of the system. Applicants believe that Schubert does not disclose this feature of the claimed invention. Applicants therefore submit that new claims 27-33 are distinctly patentable over Schubert and in condition for allowance.

CONCLUSION

In view of the above, each of the presently pending claims in this application is believed to be in condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue. If, however, the Examiner considers that further obstacles to allowance of these claims persist, we invite a telephone call to Applicants' representative.

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Respectfully submitted,

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